SN 10,029,956
Filed 12/20/01

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DEC 10 2007

PROPOSED CLAIM:

36. (Currently amended) In a plesiochronous system, a dual loop data serializer comprising:

a first-in-first-out (FIFO) register, having a fill rate, and receiving a parallel data input and a data clock input and providing a plurality of outputs;

a parallel-in serial-out (PISO) serializer having an input coupled to one of the plurality of outputs of said FIFO register, for receiving an input signal from said FIFO register, and outputting serialized data;

a phase detector, having ~~an~~ at least one input coupled to at least one of the plurality of outputs ~~an output~~ of said FIFO register, for receiving a signal representative of the fill rate of said FIFO register, said phase detector having an output for providing an output signal;

a narrow band loop filter coupled between said output of said phase detector and a phase shifter ~~having an input coupled to the output of said phase detector~~ and configured to provide an output signal to a the phase shifter, thereby producing a phase shift in a PLL;

a the phase shifter having a first input ~~coupled to~~ adapted to receive the output signal from ~~of~~ said narrow band loop filter and providing an output signal to a phase/frequency detector;

a the phase/frequency detector having an input for receiving the output signal from ~~of~~ said phase shifter and also receiving a local reference input, and providing an output signal to a wideband loop filter;

a the wideband loop filter having an input for receiving the output signal from the phase/frequency detector ~~coupled to the output of the phase/frequency detector~~ to suppress phase noise and adapted to provide ~~providing~~ an output signal to a voltage controlled oscillator (VCO);

a the voltage controlled oscillator (VCO) having an input adapted to receive coupled to the output signal from of said wideband loop filter, and providing a synthesized clock output signal to said PISO serializer and also to a second input of said phase shifter;

said phase shifter, phase/frequency detector, and wideband loop filter forming a phase locked loop with the VCO, such that the phase and frequency of the synthesized clock output signal of the VCO is modified by the output signal from of the narrow band loop filter; and

said PISO serializer providing the synthesized clock signal to said FIFO register;

whereby said phase detector compares the received data clock with the synthesized clock signal.